Transport measurements and analytical modeling of extraordinary electrical conductance in Ti-GaAs metal-semiconductor hybrid structures

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We present a comprehensive study of a phenomenon, extraordinary electroconductance (EEC), in microscopic metal-semiconductor hybrid (MSH) structures at room temperature. Our artificially designed MSH structure shows highly efficient external electric field sensing properties not exhibited by bare semiconductor structures. The microscopic device is fabricated from a GaAs epitaxial layer with a Ti/Au shunt subject to an external electric field and gives a maximum 5.2% EEC effect corresponding to an external electric field resolution of 3.05 V/cm at a bias field of 2.5 kV/cm. Moreover, the study reveals a strong dependence of the transport properties on the geometry of the MSH. An analytical two-layer model is developed which provides good agreement with the experimentally observed data. We propose that scaled down nanoscopic EEC sensor arrays can be used as an imaging technique for the charge distribution on a single cell surface in real time.

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I. INTRODUCTION

The electrical transport properties of any device depend on two factors: one physical and one geometric. The contribution to the physical components arises from the material properties such as doping level, impurities, bulk mobility, etc. On the other hand, the contribution to the geometric components comes from the configuration of the device such as the device dimensions, shape, lead contact area, lead arrangement, etc.[1] Traditionally, semiconductor device studies focused on the physical contributions and limited the geometrical effects on purpose to fully examine the underlying physics. But by careful design, the geometric contribution can be made dominant in the transport properties. The recently discovered extraordinary magnetorsistance (MR) (EMR) in a metal-semiconductor (MS) hybrid (MSH) structure by Solin *et al.*[2] is an example of geometry-driven effects. What Solin and his co-workers pointed out in the study is that the physical effects can be enhanced by geometric factors such as device shape, dimensions, and arrangements of the conducting leads. In fact, a symmetric van der Pauw (vdP) disk of homogeneous nonmagnetic InSb with an embedded concentric Au inhomogeneity exhibits a 100% MR effect at the field of 0.05 T at room temperature, exceeding the spin-dependent giant magnetoresistance (GMR) effects[3,4] and colossal MR.[5] Geometry-dependent properties, other than electronic transport, in different nanoscopic and mesoscopic devices have also been reported.[6–9]

The EMR devices have a donut shaped InSb VdP structure with a Au filling at the center. The Ohmic MS interface and the Corbino-type structure play central roles in the magnetoresistance. At zero magnetic field, the electron takes the easiest route through the metal, i.e., small effective resistance. On the other hand, at nonzero magnetic field, the Lorentz force due to the magnetic field deflects the current through the semiconductor, i.e., high effective resistance. This difference in resistance with and without the magnetic field is the origin of the geometry-dependent EMR.

By extending this general idea of geometrically driven interfacial effects on transport properties, a new class of EXX phenomena has been demonstrated, where E=extraordinary and, to date, XX=MR,[10] piezoconductance (PC),[11,12] and optoconductance (OC).[13,14]

Following the discovery of EMR, EPC, and EOC, it was realized that an electric field equivalent of the EXX phenomenon, i.e., extraordinary electroconductance (EEC), should exist, with the external electric field providing the perturbation. In principle, the EEC device should have a geometry where the external electric field redistributes the current propagation. In EMR and EOC devices, the interface between metal and semiconductor is Ohmic. Since the external electric field has very minimal or no impact on an Ohmic interface and strong effects on a Schottky MS interface, we have chosen a metal (in this case, Ti) to form a Schottky barrier at the interface. The MSH structure designed for an EEC device is shown schematically in Fig. 1(a). The Ti metal disk on top of the cylindrical GaAs mesa forms a Schottky barrier. The external electric field perpendicular to the MS interface modifies the Schottky barrier height and width, which in turn changes the current distribution through the semiconductor, i.e., changing the total resistance. This unique characteristic of the MSH design can be used in sensing efficiently the local electric field intensity. We have recently provided a proof of principle demonstration of the EEC effect in Ti-GaAs MSH structures in a brief preliminary report.[15] Here we provide the detailed experimental study of this effect and show a two-layer analytical model that quantitatively accounts for the observed transport properties under an extended range of reverse biases. We have also included a full characterization of the Schottky properties at the Ti/Au-GaAs interface.

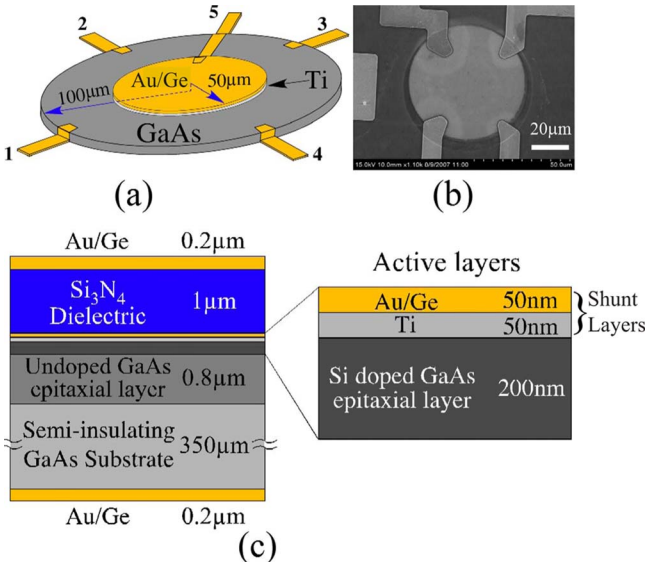

FIG. 1. (Color online) Panel (a) A three-dimensional (3D) schematic of the EEC van der Pauw structure. A concentric metal shunt of radius 50 μm is in a direct contact with the GaAs mesa of radius 100 μm. Four leads are deposited on the periphery of the mesa surface and lead 5 is directly connected to the shunt. Panel (b) An SEM image of an EEC device without the shunt metal on top. Panel (c) A cross-sectional view of the EEC multilayer structure. The shunt is composed of two 50-nm-thick metal thin films Ti and Au/Ge. A pair of parallel plates, as shown in Fig. 2, is incorporated to apply an external field with a 1 μm Si_3N_4 dielectric between the top plate and the shunt.

This paper is organized as follows. In Sec. II, we provide a detailed description of the experiment setup such as the sample preparation and the instrumentation. Then we discuss the experimental observation of different transport properties, such as the Schottky *I-V*, four-lead conductance change under electric field, device sensitivity, and resistance change under reverse shunt bias, in Sec. III. A refined two-layer analytical model developed to explain the observed transport properties is presented in Sec. IV. We compare existing field-effect devices such as junction filed effect transistor (JFETs) and metal-semiconductor field-effect transistors (FETs) (MESFETs) with our EEC devices in Sec. V. We end the paper with conclusions in Sec. VI.

II. EXPERIMENT

A. Sample design and fabrication

Our EEC devices were prepared using lattice-matched GaAs epitaxial layers, as shown in Fig. 1(c), grown by molecular-beam epitaxy (MBE). The active layer of the device is a 200-nm-thick Si-doped GaAs epitaxial layer (mobility μ=4400 $cm^2\ V^{-1}\ s^{-1}$ and carrier concentration N_D =4×10^{17} cm^{-3}) followed by an undoped 800-nm-thick epitaxially grown GaAs layer as a buffer with a semi-insulating GaAs substrate (thickness t=350 mm) at the bottom. The mesa was first fabricated using standard optical lithography and wet etching. Second, AuGe/Ni/Au metal layers for the Ohmic leads were deposited followed by a thermal annealing

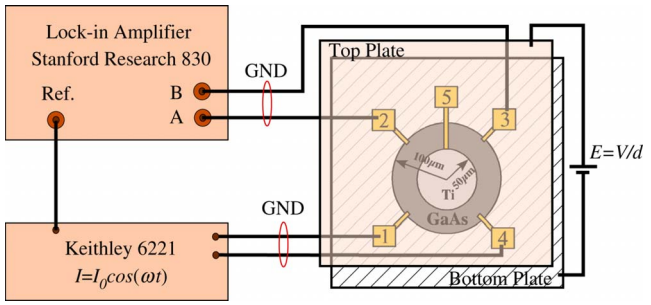

FIG. 2. (Color online) A schematic diagram of the experimental setup for measuring the four-point resistance using lock-in method. The EEC device is inside a parallel plate capacitor configuration and the electric field ($E=V/d$, where d is the separation between the top and the bottom plates) is directly proportional to the voltage applied across.

at 450 °C for 1 min. The four contacting pads of the leads are symmetrically distributed around the periphery of the mesa disk and Ohmic contacting to the surface is achieved. Next, we have deposited concentric double metal layers composed of a 50-nm-thick Ti thin film, which has an intimate contact to the GaAs epitaxial layer to form a Schottky interface, and a 50-nm-thick Au/Ge thin film, which acts as an effective shunt for electron transport. Ti and Au metals were deposited sequentially in a metal evaporation system. Before depositing metal for the Ohmic leads and the shunt, we have etched the surface oxidation by dipping the sample in an HCl:DI (1:2) solution for 5 min and by quickly transferring the sample to the evaporation system. An additional bonding lead is attached to this shunt metal for biasing purposes.

Figure 1(a) shows schematically the 3D structure of a typical EEC device. A scanning electron microscopy (SEM) image of a defined mesa connected with four Ohmic leads is shown in Fig. 1(b). To test our device under an external electric field, a pair of capacitor plates is incorporated into the EEC structure. In order to prevent leakage current from the top metal plate to the Au/Ge shunt, a 1-μm-thick layer of Si_3N_4 is sandwiched in between. The Si_3N_4 insulating dielectric was deposited by plasma-enhanced chemical vapor deposition (PECVD) and etched with a plasma etcher. A schematic cross-sectional view of the heterostructure is shown in Fig. 1(c). Finally we have deposited the two metal layers of AuGe for the top and bottom capacitor plates, as shown in Fig. 2, using optical lithography.

We define a geometrical parameter α to be the ratio of the shunt radius r_s to the mesa radius r_m. As in Fig. 1(a), r_s =50 μm and r_m=100 μm, i.e.,

$$\alpha = \frac{r_s}{r_m}. \tag{1}$$

Two sets of devices with r_m=100 and 60 μm have been studied and each set contains 15 devices with α from 0/16 (controlled sample) to 14/16.

B. Experimental setup

Before testing the EEC effect, the property of the Schottky interface needs to be characterized. The four Ohmic leads are numbered from 1 to 4 clockwise and the lead to the shunt is numbered as 5 as shown in the Fig. 1(a). By attaching the shunt lead 5 and ground lead 4 to a current source (Keithley 6221) and a nanovoltmeter (Keithley 2182) in parallel, the *I-V* characteristics can be obtained. With the Si_3N_4 dielectric between the top capacitor plate and the shunt metal, the resistance is found to be $\sim 10^{12}$ Ω, which assures negligible current leakage through the MS interface in the device.

The EEC device contains a van der Pauw[16] mesa structure. The resistance of the device was measured in a four-probe setup to eliminate any influence of the contact resistance between the metal leads and semiconductor. In addition, we adopted both the delta method[17] and lock-in method[18] to measure the resistance to exclude low-frequency ($f < 100$ Hz) thermal noise. In the delta method, a Keithley 6221 provides a square-wave current with amplitude of 20 μA at a frequency of 0.2 kHz. A Keithley 2182 performs A/D conversion at source high and source low points. A three-point moving-average algorithm is used to calculate the four-lead resistance. In the lock-in method, as shown schematically in Fig. 2, the square-wave current is replaced with a sinusoidal wave at the frequency of 7 kHz and the data were sampled uniformly along the oscillation. As both methods produce equivalent results, we chose the lock-in method due to its faster data acquisition. The external electric field is realized by applying a dc voltage across the top and bottom capacitor plates built into the device. All the measurements were carried out at room temperature. The EEC device and electrical feedthroughs were enclosed in a grounded metal box to isolate the measurement from the external noise or disturbance.

III. EXPERIMENTAL OBSERVATIONS

A. Schottky *I-V*

The main panel of Fig. 3 shows the Schottky rectification property originating from the Ti-GaAs MS interface. Here the Schottky *I-V* characteristic is measured between the terminals 5 and 4 as shown in Fig. 1(a). Ti adheres well to GaAs and the Ti-GaAs interface forms an excellent Schottky barrier.[19] We have measured the Schottky *I-V* curve for 60 devices and all showed similar characteristics to those presented in Fig. 3. In the reverse bias region ($V < 0$), the current is essentially zero before breaking down, while in the forward bias region ($V > 0$), the current increases sharply after a threshold voltage V_T, where $V_T \sim 0.3$ V.

For a metal-semiconductor system with a moderately doped semiconductor ($5 \times 10^{16} \leq N_D \leq 5 \times 10^{17}$ cm^{-3}), as in the EEC devices, the tunneling of thermally excited electrons or thermionic field emission (TFE) dominates the electron transport. The total current can be expressed as[20]

$$I = I_s[\exp(qV/nkT) - 1], \tag{2}$$

where q is the electron charge and I_s is the saturation current, a complicated function of the MS interfacial area, barrier height, properties of the semiconductor, and the operation temperature. It can be obtained by extrapolating the current from the linear extension of ln *I-V* at $V=0$. Here n is the so-called ideal factor and is defined as

$$n \equiv \frac{q}{kT}\frac{\partial V}{\partial(\ln J)}, \tag{3}$$

where J is the current density. The deviation of a real Schottky interface from the ideal ($n=1$) can be attributed to many effects, such as electron trapping and recombination,[21] barrier inhomogeneities,[22] an interfacial oxide layer,[23] image force lowering,[24] shunt resistance,[25] and series resistance.[26] In the two-terminal Schottky *I-V* measurement, comparing to an ideal Schottky diode, the EEC device has a built-in series resistance. When a current is sent from lead 5 to 4, it passes through the Schottky interface as well as the annular-shaped GaAs uncovered by metal, which leads to a series resistance. When the current is in the high forward bias regime, i.e., $I > 16$ μA, the term "−1" in Eq. (2) is negligible. To incorporate the effect of the series resistance, Eq. (2) can be modified as

$$I = I_s \exp[q(V - IR_{se})/n_0 kT] \tag{4}$$

where R_{se} is the series resistance and n_0 is the modified ideal factor of the diode excluding the effect from R_{se}. By taking the natural logarithm of Eq. (4), differentiating both sides by $d/d \ln I$, and plugging in Eq. (3), we have

$$n = n_0 + (qR_{se}/kT)I. \tag{5}$$

Thus the series resistance leads to a linear dependence between the ideal factor n and the current I, which is shown in inset (a) of Fig. 3. From the intercept and the slope, n_0

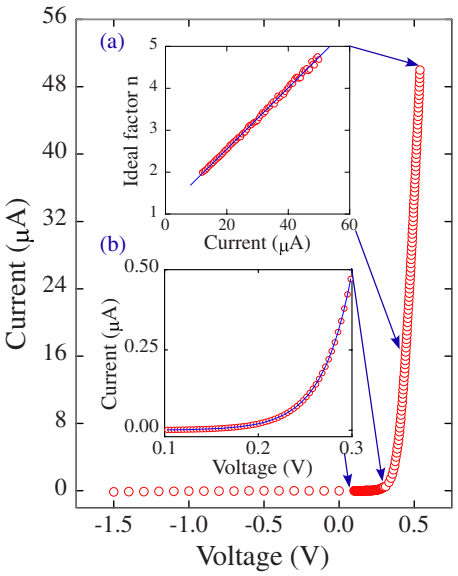

FIG. 3. (Color online) Main panel: the room-temperature *I-V* characteristic of the Schottky interface. The inset (a) shows the linear dependence between the ideal factor n and the current as $I < 16$ μA. The inset (b) shows the quasiexponential dependence between the current and the voltage as $0 < I < 0.5$ μA. Lines are the curve fittings.

$=1.142$ and $R_{se}=1818\ \Omega$ can be obtained, respectively. In fact, R_{se} can be estimated from a simple approximation, where the current from lead 5 to 4 is assumed to be highly concentrated in a rectangular-shaped channel within the uncovered region of the GaAs mesa. The channel length is (r_m-r_s) and the width is the same as the contact pads, i.e., 4 μm, while the channel height equals to the mesa thickness, i.e., 200 nm. The resistivity of the GaAs can be calculated from the carrier mobility and concentration. The result is $\sim 1400\ \Omega$. As both numbers are on the same order of magnitude, the above two calculations are self-consistent. In addition, if we directly fit ln *I*-*V* from Eq. (2) with a straight line, $n\sim 1.31$. As n_0 is much closer to 1 than n, this confirms the notion that R_{se} induces nonideal properties to the EEC Schottky interface.

At a low forward bias $0<I<0.5\ \mu$A, the effect from R_{se} is minimal as $IR_{se}\ll V$ and the shunt effect becomes important. The current starts to bypass the Schottky barrier through a shunt resistance R_{sh} and Eq. (2) is further modified as

$$I = I_s[\exp(qV/n_0'kT) - 1] + V/R_{sh}. \tag{6}$$

Here to distinguish it from n_0, n_0' is used as the modified ideal factor excluding the shunt effect. In the low current bias regime $0<I<0.5\ \mu$A, an exponential-linear combination function $y=p_1e^{-x/p_2}+p_3+p_4x$ fits the data perfectly. The two parameters in Eq. (6), $R_{sh}=3.45\times 10^8\ \Omega$ and $n_0'=1.197$, can be extracted from the fitting parameters p_4 and p_2, respectively. Inset (b) of Fig. 3 shows the quasiexponential *I*-*V* dependence in this region. The characterization of the shunt resistance in an EEC device is crucial to the understanding of the electron-transport property under an electric field. In addition to the Schottky barrier, the shunt resistance provides another path for electrons from the GaAs mesa to get access to the Ti/Au shunt and results in a redistribution of the current between the metal and the semiconductor. This current redistribution gives rise to a measurable device conductance change.

B. EEC four-lead resistance under direct bias

We measure the device resistance by sending a current through leads 1 and 4, I_{14} and measuring the voltage drop across leads 2 and 3, V_{23}. The observed resistance R_{obs} is given by

$$R_{obs}(\alpha,E) = \frac{1}{G(\alpha,E)} = \frac{V_{23}}{I_{14}}, \tag{7}$$

where $G(\alpha,E)$ is the sample conductance. Using an electric field, we can externally perturb the EEC device in two different ways. First is by applying a bias voltage across the shunt lead 5 and the ground lead 4, which we label as direct biasing. The nonlinear current-voltage dependence and the nonuniform field distribution at the MS interface make it very complicated to calculate the local-field intensity. Second is by applying a bias voltage across the capacitor's top and bottom plates, which we label as indirect biasing. The field intensity in this case is simply given by $E=V/d$, where d ($\sim 400\ \mu$m for the EEC devices studied here) is the separation between the top and bottom plates. Under a direct bias, the EEC device operates as a field-effect transistor (FET). The direct bias voltage ranges from -2 to $+1$ V, as shown in Fig. 4. In the reverse bias region, sample resistance declines linearly as the bias increases (i.e., the magnitude of bias voltage decreases), and this linear dependence continues into the forward region until $V\sim V_T$ followed by a dramatic drop in the device resistance.

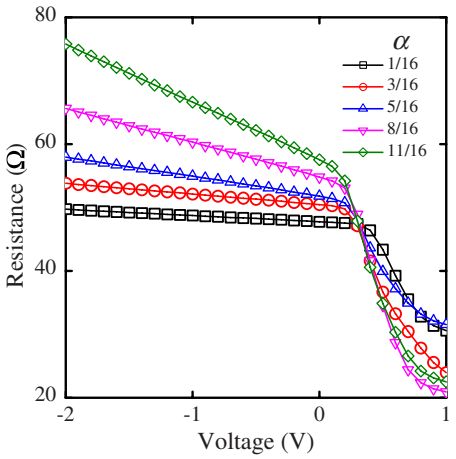

FIG. 4. (Color online) The four-lead resistance of samples with 60 μm in mesa radius and different values under direct bias voltage.

The rapid decrease in resistance in the forward bias region arises from current injection. When a metal and an *n*-type semiconductor have an intimate contact, electrons from the semiconductor conduction-band flow into the metal until the Fermi levels on the two sides line up. Positive ionized donors are left behind in the semiconductor while electrons that surmount or tunnel through the barrier form a thin sheet of negative charges on the metal surface. An internal electric field from semiconductor to metal is built up. As electrons move out of the semiconductor into the metal, the free-electron concentration near the boundary decreases and a high-resistivity depletion region is formed. The depletion width W depends on the square root of the applied bias voltage.[27] When a forward bias is applied, the resultant electric field at the interface decreases and so does the depletion width. For the devices shown in Fig. 4, when V increases to $+0.3$ V, the depletion is thin enough for a large number of electrons to tunnel through the barrier leading to a substantial decrease in the measured four-lead resistance. Therefore, the depletion width at equilibrium, W_0, can be estimated from this threshold voltage, which will be discussed in Sec. IV A.

C. EEC four-lead resistance under external electric field and its field sensitivity

The EEC devices are essentially field-controlled resistors, which can be used as electric field sensors. To study the response of our devices to an external electric field, a quantity *EEC* is defined to be the percentage change in sample conductance with an external electric field and without field and is given by

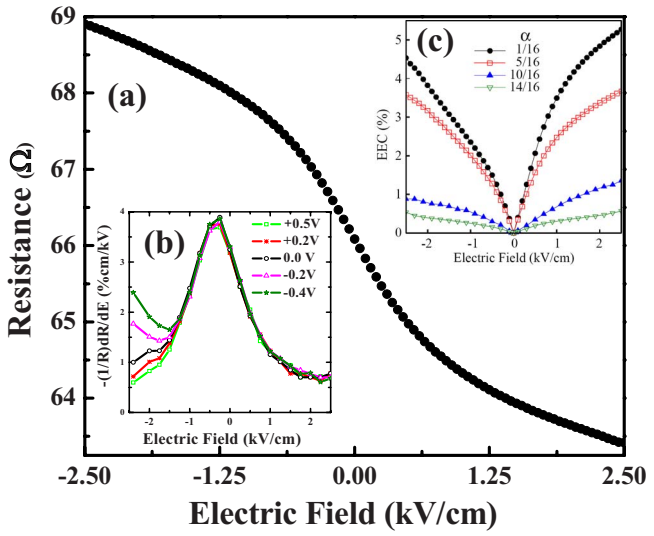

FIG. 5. (Color online) Main panel (a) Four-point resistance of an EEC device measured with respect to an external electric field. Inset (b) shows the device sensitivity at the corresponding shunt biases. Panel (c) EEC effects in four different devices with $\alpha = 1/16, 5/16, 10/16, 14/16$.

$$EEC = \frac{|G(\alpha,E) - G(\alpha,0)|}{G(\alpha,0)} \times 100\%, \tag{8}$$

where α is the geometric factor defined in Eq. (1) and $G(\alpha,E)$ is the sample conductance defined in Eq. (7).

To test the EEC effect, we connect the top and bottom metal plates to a voltage source (Keithley 230) to supply a static field using a dc voltage. Compared to the internal field at the MS interface, usually between 10^5 and 10^6 V/cm, the applied field ($\sim 10^3$ V/cm) is very small and can be treated as a perturbation. Figure 5(a) shows the field effect on the four-lead resistance of an EEC device under zero shunt bias. For example, as the field increases from −2.5 to +2.5 kV/cm, the sample resistance at zero shunt bias decreases continuously from 69 to 63.5 Ω. Thus the measured four-lead resistance is a figure of merit for electric field sensing.

We calculate the device sensitivity as the percentage change in sample conductance with respect to the field change, i.e., $[1/G](dG/dE) \times 100\%$. The optimum value is found to be independent of the shunt bias V_B and is an intrinsic property of the device. The inset of Fig. 5(b) shows the sensitivity of an EEC device with $r = 100$ μm and $\alpha = 1/16$ under five different shunt biases. For $E > -1$ kV/cm, the sensitivity of the device is independent of V_B. As a result, shunt lead 5 is optional for the optimized EEC sensors and its removal will simplify the design and fabrication of EEC nanosensors and arrays by reducing 1/5 of the total pin outs and connecting circuits.

Our EEC devices are fundamentally different from a regular Schottky diode. For EEC devices, the shunt metal forming the Schottky barrier does not need to be externally connected. On the other hand, a regular Schottky diode is a two-terminal device, where the metal and the semiconductor are connected to external terminals.

Using the instrument precision values and the EEC device sensitivity, one can determine the sensor resolution or the smallest detectible field. For a typical four-lead resistance test, the magnitude of the alternating current is 20 μA with a precision of 1 nA. During the test, the lock-in amplifier provides a reading of 0.8982 mV with an accuracy of 0.1 μV. Since the error propagates as $\left|\frac{\Delta R}{R}\right| = \sqrt{\left(\frac{\Delta I}{I}\right)^2 + \left(\frac{\Delta V}{V}\right)^2}$, the field resolution can be expressed as $\frac{|\Delta R/R|}{\text{sensitivity}} = 3.05$ V/cm at the sensitivity of 4%, or in other words, the smallest field that this EEC sensor can detect is 3.05 V/cm.

Figure 5(c) demonstrates the geometrical dependence of the EEC effect. Under +2.5 kV/cm, a maximum of 5.2% EEC effect is obtained in a device with $r_m = 100$ μm and $\alpha = 1/16$. Comparing the four devices presented in Fig. 5(c), it is interesting to note that the smaller the geometrical parameter α, the larger the effect. With the same mesa size, a device with a smaller α has a smaller interfacial area, yet a larger ratio between the periphery and the area of the metal shunt disk, i.e., $2\pi/r_s$. Along the edge of the metal disk, the local electric field at the MS interface is much larger than the interior due to an accumulation of surface charges. Under a uniform electric field, the region of high surface charge concentration is more sensitive to the applied field than the region of low charge concentration. Therefore, the EEC device with $\alpha = 1/16$ exhibits the largest percentage change in conductance compared to other devices with larger α. A 3D finite-element simulation of the dynamic interfacial charge distribution is in progress to interpret the geometry dependence of the EEC effect quantitatively.

IV. ANALYTICAL MODELING

A. Field dependence of the depletion width

The potential in the semiconductor space-charge region of a Schottky system can be described by the Poisson equation

$$-\frac{d^2V}{dz^2} = \frac{\rho(z)}{\epsilon_s} \quad (0 < z < W), \tag{9}$$

where ϵ_s is the permittivity of GaAs, W is the depletion width, and z is the vertical distance from MS interface shown in Fig. 6(a). For a typical MS system, a uniformly doped semiconductor and an abrupt change in space-charge density at the depletion boundary are assumed. The internal electric field strength increases linearly with distance $(W-z)$ from the depletion boundary and peaks at the MS interface. By solving the Poisson equation under the above boundary conditions, one can show that[27]

$$W = \sqrt{\frac{2\epsilon_s}{qn}\left(V_{\text{in}} - V_B - \frac{kT}{q}\right)}, \tag{10}$$

where V_{in} is the built-in potential and V_B is the applied bias voltage. At equilibrium or $V_B = 0$ V, Eq. (10) yields $W_0 = 31.5$ nm for EEC devices with $V_{\text{in}} = 0.3$ V.

B. Two-layer model

Under a reverse bias, the depletion region expands and little current can flow across the MS interface. Therefore, the

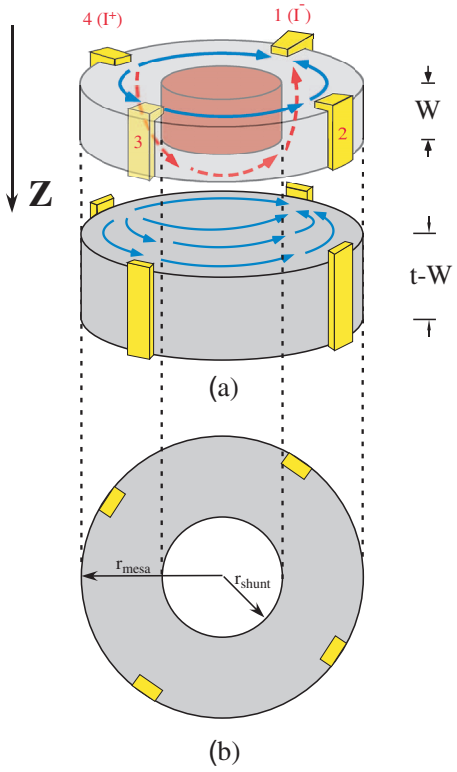

FIG. 6. (Color) Panel (a) A 3D schematic of the two-layer structure when the EEC device is under a reverse bias. The red cylinder in the top layer represents the depletion region. The blue arrows in both layers correspond to the in-plane current considered in calculating the resistance of the EEC device. The dashed red arrow in the top layer shows the nonlaminar current that flows from the top annulus region to the bottom layer underneath the depletion region. Panel (b) The top view of the upper layer in the two-layer model. The center inhomogeneity has the same radius as the metal shunt and the same thickness as the depletion width.

semiconductor is effectively separated from the metal by the depletion layer and can be modeled individually. The four-lead resistance essentially consists of two GaAs thin-film layers connected in parallel, a GaAs annulus of thickness W, and a GaAs cylinder of thickness $t-W$, as shown in Fig. 6(a). The concentric hole on the top layer, with a radius of r_s and a thickness of W, corresponds to the depletion region.

The apparent resistivity of a cylindrically symmetric van der Pauw configuration of radius $r=a$ with a conducting inhomogeneity of radius $r=b$ is given by[28,29]

$$\rho_{\text{app}} = \frac{1}{\sigma \ln 2} \sum_{p=1}^{\infty} \left[\frac{2(1-\gamma\alpha^{2p})}{(1+\gamma\alpha^{2p})} - \frac{(1-\gamma\alpha^{4p})}{(1+\gamma\alpha^{4p})} \right] \frac{1}{p} (-1)^{p+1}, \tag{11}$$

where

$$\gamma = \frac{(\sigma_0^2 - \sigma^2)}{(\sigma_0 + \sigma)^2} = \frac{\beta^2 - 1}{(\beta+1)^2}. \tag{12}$$

Here $\alpha=b/a$ and $\beta=\sigma_0/\sigma$. σ and σ_0 are the conductivity of the medium and the inhomogeneity respectively. In the two-layer model, α varies from 1/16 to 14/16 with $b=r_s$ and $a=r_m$ according to Eq. (1). The parameter β represents the accessibility of the current through the depletion region. $\beta=0$ represents a completely depleted inhomogeniety medium, i.e., no current flowing through the inhomogeniety medium. On the other hand, $\beta=1$ corresponds to no depletion, i.e., the current transport is similar to the semiconductor region. To determine that value of β for our EEC devices, we have compared the experimentally measured four-point resistance to the values calculated from the two-layer model for different β's as shown in Fig. 7. The excellent agreement of the measured values to the values for $\beta=0$ suggests that negligible current is flowing through the inhomogeneity region for our EEC devices. Hence we can safely assume that $\sigma_0=0$ or $\gamma\rightarrow-1$. When n becomes fairly large, $\alpha^{2n}\rightarrow 0$ as $\alpha<1$. Thus the series converges to $(-1)^{n+1}/n$ and the sum is calculated numerically.

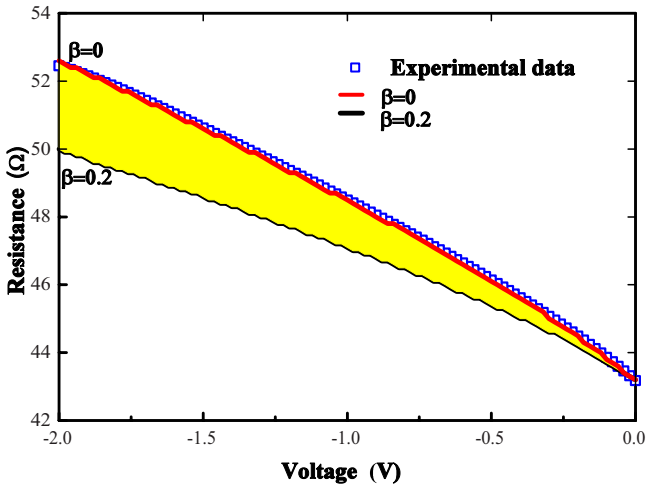

FIG. 7. (Color online) The comparison of the curvature between the measured four-point resistance of the EEC device of $\alpha=7/16$ and the values calculated from the two-layer analytical model for different β's. The shaded area corresponds to the lines for different values of β ranging from 0 (top) to 0.2 (bottom). We have added offset values of −12.02 and +1 Ω from the measured resistance and $\beta=0.2$ lines, respectively, so that the plotted lines converge at the zero voltage ($V=0$).

For the bottom GaAs cylinder, the apparent resistivity ρ_{app} is simply the inverse of the medium conductivity $(1/\sigma)$, as $\alpha=0$ and $\Sigma_{n=1}^{\infty}(-1)^{n+1}/n=\ln 2$. The measured four-lead resistance and the apparent resistivity are related by the van der Pauw expression[16]

$$\rho_{\text{app}} = \frac{\pi t}{\ln 2} \frac{V_{23}}{I_{14}}. \tag{13}$$

Based on the two-layer model, the measured resistance $R(\alpha, V_B)$ can be calculated as follows:

$$\frac{1}{R(\alpha, V_B)} = \frac{1}{R_{\text{top}}(\alpha, V_B)} + \frac{1}{R_{\text{bottom}}(V_B)}, \tag{14}$$

where

$$R_{\text{top}} = \frac{1}{\pi\sigma W}\sum_{p=1}^{\infty}\left[\frac{2(1+\alpha^{2p})}{(1-\alpha^{2p})} - \frac{(1+\alpha^{4p})}{(1-\alpha^{4p})}\right]\frac{1}{p}(-1)^{p+1} \tag{15}$$

and

$$R_{\text{bottom}} = \frac{\ln 2}{\pi\sigma(t-W)}. \tag{16}$$

One interesting implication from Eqs. (11) and (13) is that the measured resistance does not depend on either the mesa radius or the shunt radius individually, but on the radius ratio. If the model properly describes reality, EEC nanosensors with a fixed α will have the same field sensitivity yet provide a much higher spatial resolution than the microscopic sensors studied in this paper.

C. Theory and experimental comparison

Before comparing to the experiment, two approximations in the model need to be addressed. First, the voltage and current probes of an EEC device use surface contacts whereas the model assumes sidewall contacting. Thus, in the experiment, the current flow underneath the metal contact pads 1 and 4 is perpendicular to the mesa surface. The electrons that reach the bottom layer, i.e., the cylindrical GaAs, must have passed through the top annulus GaAs layer. This nonlaminar current flow introduces additional series resistance in the measurement compared to the sidewall-contacting model. Second, the current I_{14} inside the semiconductor layer has a 3D distribution and electrons from the top layer may take the route under the center inhomogeneity (depletion region) and flow through the bottom layer, as shown in Fig. 6(a). In contrast, the model describes in-plane electron flow in parallel with no disruptions between layers.

The above two approximations suggest that the experimentally observed resistance will be consistently larger than the analytical prediction from Eq. (14). To account for this discrepancy, an adjustable parameter $R_C(\alpha)$ is used,

$$R'(\alpha, V_B) = R(\alpha, V_B) + R_C(\alpha). \tag{17}$$

Here $R'(\alpha, V_B)$ is the adjusted resistance predicted by the two-layer model and V_B is the direct bias voltage applied across the leads 5 and 4.

For clarity of presentation, Fig. 8 compares the theoretical prediction $R(\alpha, V_B)$ [Eq. (14), solid lines] and the adjusted experimental results $[R_{\text{obs}} - R_C(\alpha)]$ [Eqs. (7) and (17), symbols]. The model provides a good fit to the data for various values of V_B and α. The values of $R_C(\alpha)$ are given in the caption of Fig. 8. The quality of this one-parameter fitting for α in the middle range, i.e., from 4/16 to 10/16, is better than those for α close to 0 or 1. When α is small, the effect from the high charge density along the metal shunt edge becomes important and impacts the resistance response to the bias voltage. On the other hand, as α approaches 1, the surface contact pads are so close to the metal shunt, which makes the current path more complicated in the real device than what the model predicts. We have fit the data only in the reverse bias direction with $-2 < V_B < 0$ V. Under a forward bias, the depletion region is diminished and electrons flow through the MS interface. As electrons get access to the metal shunt, the two-layer structure is inadequate for modeling the current transport within the MSH.

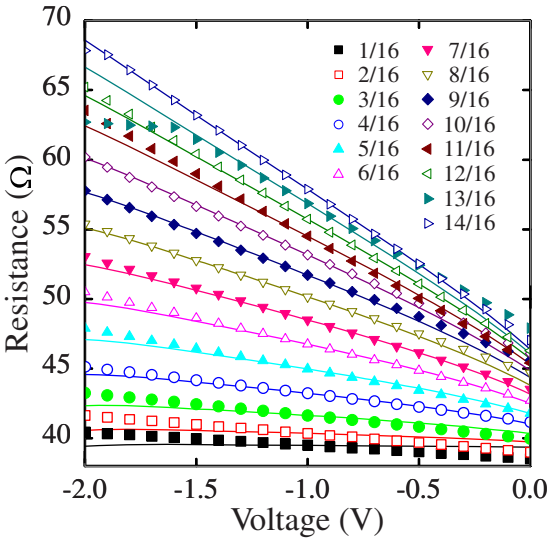

FIG. 8. (Color online) The comparison between theory and experiment on the four-lead resistance of samples with 60 μm in mesa radius and a full spectrum of values under direct reverse bias. The solid lines are theoretical predictions from the two-layer model with the adjustable parameter $[16\alpha, R_C(\alpha)] = (1, 10.92\ \Omega)$, $(2, 20.45\ \Omega)$, $(3, 12.69\ \Omega)$, $(4, 6.09\ \Omega)$, $(5, 11.23\ \Omega)$, $(6, 13.63\ \Omega)$, $(7, 12.02\ \Omega)$, $(8, 9.39\ \Omega)$, $(9, 7.81\ \Omega)$, $(10, 6.91\ \Omega)$, $(11, 13.22\ \Omega)$, $(12, 9.16\ \Omega)$, $(13, 10.97\ \Omega)$, and $(14, 13.39\ \Omega)$.

V. COMPARISON BETWEEN EEC AND JFET OR MESFET

When a direct reverse bias is applied between leads 5 and 4 with no voltage across the capacitor plates, an EEC device behaves like a JFET (Ref. 30) or a MESFET.[20] Under this operating mode, the fundamental difference between the two types of device comes from the geometry. In EEC devices, the metal shunt radius varies with the mesa radius fixed and the radius ratio α changes from 1/16 to 14/16. The four-lead resistance has a clear dependence on the geometrical parameter α as shown in Fig. 8. In contrast, for most JFETs and MESFETs, the metal gates have fixed sizes and thus the gate size dependence of the characteristic I_D-V_D in FETs has never been studied.

Other than the geometry, the EEC effect distinguishes itself from the FETs by the forward field effect, as the JFETs and MESFETs are normally operated under reverse biases. For an EEC device, under a forward electric field, the depletion is thinned and more thermally excited electrons tunnel through the barrier near the top from semiconductor to metal. The Ti and Au/Ge thin films act as both a Schottky gate and a current shunt. By providing an alternative route for electrons traveling from semiconductor to metal, current paths are not restricted to the conducting channels shaped by the depletion region. This contributes significantly to the geometry dependence of the EEC effect.

VI. SUMMARY

We have successfully designed, fabricated, and modeled another type of electric field sensor. A van der Pauw disk of homogeneous GaAs with a concentric Au/Ti disk on top is found to exhibit room-temperature electroconductance of 5.2% at an electric field of 2.5 kV/cm. With the current testing system, the sensor resolution is 3.05 V/cm. The two-layer model successfully predicts the linear dependence between the reverse bias voltage and four-lead resistance and fits the measured resistance quite well. In a real-life application, EEC sensors may be scaled down to the nanoregime and assembled into sensor arrays. By measuring the local electric field intensity at very high spatial resolution, one might construct a charge distribution image on a cell surface in real time.

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